Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A transistor comprising:

a ferromagnetic source that is formed with a ferromagnetic body from which spin-polarized conduction carriers are injected;

a ferromagnetic drain that is formed with a ferromagnetic body that receives the spin-polarized conduction carriers injected from the ferromagnetic source;

a semiconductor layer that is provided between the ferromagnetic source and the ferromagnetic drain, and forms a Schottky junction having a Schottky barrier at each junction interface with the ferromagnetic source and the ferromagnetic drain; and

a gate electrode that is formed associated with the semiconductor layer,

wherein the Schottky barrier appears on the conduction band side when the spin-polarized conduction carriers are electrons, and the Schottky barrier appears on the valence band side when the spin-polarized conduction carriers are holes, with the spin-polarized conduction carriers being of the same conduction type as that of the semiconductor layer (an accumulation channel type).

2. (Original) The transistor as claimed in claim 1, wherein the magnetization direction of the ferromagnetic source or the ferromagnetic drain is inverted, so that the relative magnetization direction of the ferromagnetic drain is made equal ("parallel magnetization") to or opposite ("antiparallel magnetization") to the magnetization direction of the ferromagnetic source.

3. (Original) The transistor as claimed in claim 1, wherein the ferromagnetic source and the ferromagnetic drain are made of a ferromagnetic metal.

4. (Canceled)

5. (Previously Presented) A transistor comprising:

a ferromagnetic source that is formed with a ferromagnetic body from which spin-polarized conduction carriers are injected;

a ferromagnetic drain that is formed with a ferromagnetic body that receives the spin-polarized conduction carriers injected from the ferromagnetic source;

a semiconductor layer that is provided between the ferromagnetic source and the ferromagnetic drain, and forms a Schottky junction having a Schottky barrier at each junction interface with the ferromagnetic source and the ferromagnetic drain; and

a gate electrode that is formed associated with the semiconductor layer,

wherein the Schottky barrier appears on the valence band side when the spin-polarized conduction carriers are electrons, and the Schottky barrier appears on the conduction band side when the spin-polarized conduction carriers are holes, with the spin-polarized conduction carriers being of a different conduction type from that of the semiconductor layer (an inversion channel type), the semiconductor layer not having an inversion layer formed therein.

6. (Previously Presented) The transistor as claimed in claim 1, wherein, with a voltage not being applied between the gate electrode and the ferromagnetic source, the Schottky barrier restrains the spin-polarized conduction carriers from being injected to the semiconductor layer due to tunneling and heat radiation, the transistor being of the accumulation channel type.

7. (Previously Presented) The transistor as claimed in claim 1, wherein a voltage is applied to the gate electrode, so that the spin-polarized conduction carriers of the ferromagnetic source are injected to the semiconductor layer by tunneling the Schottky barrier at the interface between the ferromagnetic source and the semiconductor layer, the transistor being of the accumulation channel type.

8. (Previously Presented) The transistor as claimed in claim 1, wherein, with a voltage not being applied to the gate electrode, the Schottky barrier restrains the spin-polarized conduction carriers from being injected to the semiconductor layer due to heat radiation, while the spin-polarized conduction carriers of the ferromagnetic source are injected to the semiconductor layer by tunneling the Schottky barrier, the transistor being of the accumulation channel type.

9. (Previously Presented) The transistor as claimed in claim 1, wherein, with a voltage being applied to the gate electrode, the spin-polarized conduction carriers of the ferromagnetic source tunnels the Schottky barrier at the interface between the ferromagnetic source and the semiconductor layer, so as to control a current that is generated between the ferromagnetic source and the ferromagnetic drain, the transistor being of the accumulation channel type.

10. (Original) The transistor as claimed in claim 5, wherein, with a voltage not being applied between the gate electrode and the ferromagnetic source, the Schottky barrier restrains the spin-polarized conduction carriers from being injected to the semiconductor layer due to tunneling and heat radiation, the transistor being of the inversion channel type.

11. (Original) The transistor as claimed in claim 5, wherein a voltage is applied to the gate electrode to form an inversion layer in the semiconductor layer, so that the spin-polarized conduction carriers of the ferromagnetic source are injected to the semiconductor layer due to at least one of heat radiation and tunneling, the transistor being of the inversion channel type.

12. (Original) The transistor as claimed in claim 5, wherein, even with a voltage not being applied to the gate electrode, an inversion layer is formed in the semiconductor layer, and the spin-polarized conduction carriers of the ferromagnetic source are injected to

the semiconductor layer due to at least one of heat radiation and tunneling, the transistor being of the inversion channel type.

13. (Original) The transistor as claimed in claim 5, wherein, with a voltage being applied to the gate electrode, the spin-polarized conduction carriers of the ferromagnetic source are injected from the ferromagnetic source to the semiconductor layer due to at least one of heat radiation and tunneling, so as to control a current generated between the ferromagnetic source and the ferromagnetic drain, the transistor being of the inversion channel type.

14. (Previously Presented) The transistor as claimed in claim 1, wherein the spin-polarized conduction carriers injected to the semiconductor layer are spin-polarized in accordance with the spin polarization rate at the Fermi energy of the ferromagnetic source, the transistor being of the accumulation channel type.

15. (Previously Presented) The transistor as claimed in claim 1, wherein:

when the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is parallel magnetization, an electric resistance due to spin-dependent scattering of the spin-polarized conduction carriers injected from the ferromagnetic source is low in the ferromagnetic drain;

when the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is antiparallel magnetization, the electric resistance due to spin-dependent scattering of the spin-polarized conduction carriers injected from the ferromagnetic source is high in the ferromagnetic drain,

the transistor being of the accumulation channel type.

16. (Previously Presented) The transistor as claimed in claim 1, wherein transconductance can be controlled in accordance with the relative magnetization direction of

the ferromagnetic drain with respect to the ferromagnetic source, with the same bias being applied.

17. (Previously Presented) The transistor as claimed in claim 1, wherein, when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, the transistor has a threshold voltage that is defined as a gate voltage for generating a predetermined current between the ferromagnetic source and the ferromagnetic drain, with a voltage being applied to the gate electrode,

the transistor being of the accumulation channel type.

18-39. (Canceled)

40. (Original) The transistor as claimed in claim 1, wherein the ferromagnetic source and the ferromagnetic drain are formed through growth or deposition on the semiconductor layer.

41. (Original) The transistor as claimed in claim 1, wherein the ferromagnetic source and the ferromagnetic drain are by introducing magnetic elements into the semiconductor layer.

42. (Previously Presented) A memory device comprising

the transistor as claimed in claim 1,

using the transistor, information being stored in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source,

the information stored in the transistor being detected based on the transconductance of the transistor depending on the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source.

43. (Original) A memory device comprising:

the transistor as claimed in claim 1;

a first line that is connected to the gate electrode;

a second line that is connected to the ferromagnetic drain; and

a third line that grounds the ferromagnetic source.

44. (Original) A memory device comprising:

the transistor as claimed in claim 1;

a first line that is connected to the gate electrode;

a second line that is connected to the ferromagnetic drain;

a third line that grounds the ferromagnetic source;

an output terminal that is formed at one end of the second line; and

a fourth line that branches from the second line and is connected to a power source via a load.

45. (Original) The memory device as claimed in claim 43, further comprising

a first extra line and a second extra line that cross each other on the transistor or in the vicinity of the transistor, being electrically insulated.

46. (Original) The memory device as claimed in claim 43, wherein the first extra line and the second extra line, or one of the first extra line and the second extra line is replaced with the first line and the second line, or one of the first line and the second line.

47. (Original) The memory device as claimed in claim 45, wherein the magnetization of the ferromagnetic source or the ferromagnetic drain is inverted by a magnetic field that is induced by applying a current to the first extra line and the second extra line, or the first line and the second line that replace the first extra line and the second extra line, or one of the first line and the second line that replaces one of the first extra line and the second extra line and the other one of the first extra line and the second extra line that is not replaced, so that the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is changed to rewrite information.

48. (Original) The memory device as claimed in claim 43, wherein:

when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, a voltage that is higher than the threshold voltage is applied to the first line; and

information is read out, based on the size of a drain current at the transistor when a predetermined bias is applied between the ferromagnetic source and the ferromagnetic drain.

49. (Original) The memory device as claimed in claim 44, wherein information is read out with an output voltage that is obtained based on a voltage drop due to the load caused by a drain current generated at the transistor when a voltage higher than the threshold voltage is applied to the gate electrode via the first line, the ferromagnetic source and the ferromagnetic drain exhibiting parallel magnetization.

50. (Original) A memory circuit comprising:

the transistors as claimed in claim 1, the transistors being arranged in a matrix fashion;

first lines that ground the respective ferromagnetic sources;

a plurality of word lines that connect the respective gate electrodes of the transistors that are arranged in the column direction; and

a plurality of bit lines that connect the respective ferromagnetic drains of the transistors that are arranged in the row direction.

51. (Original) A memory circuit comprising:

the transistors as claimed in claim 1, the transistors being arranged in a matrix fashion;

first lines that ground the respective ferromagnetic sources;

a plurality of word lines that connect the respective gate electrodes of the transistors that are arranged in the column direction;

a plurality of bit lines that connect the respective ferromagnetic drains of the transistors that are arranged in the row direction;

output terminals each formed at one end of each of the bit lines; and

second lines that branch from the respective bit lines and are connected to a power source via a load.

52. (Original) The memory circuit as claimed in claim 50, further comprising

a first extra line and a second extra line that crosses each other on each of the transistors or in the vicinity of each of the transistors, the first extra line and the second extra line being electrically insulated.

53. (Original) The memory circuit as claimed in claim 52, wherein the first extra line and the second extra line, or one of the first extra line and the second extra line is replaced with the corresponding word line and the corresponding bit line, or one of the corresponding word line and the corresponding bit line.

54. (Original) The memory circuit as claimed in claim 50, wherein the magnetization of the ferromagnetic source or the ferromagnetic drain is inverted by a magnetic field that is induced by applying a current to the first extra line and the second extra line, or the word line and the bit line that replace the first extra line and the second extra line, or one of the word line and the bit line that replaces one of the first extra line and the second extra line and the other one of the first extra line and the second extra line that is not replaced, so that the relative magnetization state between the ferromagnetic source and the ferromagnetic drain is changed to rewrite information.

55. (Original) The memory circuit as claimed in claim 50, wherein:

when the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization, a voltage that is higher than the threshold voltage is applied to the word line; and

information is read out, based on the size of a drain current at the transistor when a predetermined bias is applied between the ferromagnetic source and the ferromagnetic drain.

56. (Original) The memory circuit as claimed in claim 51, wherein information is read out with an output voltage that is obtained based on a voltage drop due to the load caused by a drain current generated at the transistor when a voltage higher than the threshold voltage is applied to the gate electrode via the word line, the ferromagnetic source and the ferromagnetic drain exhibiting parallel magnetization.

57. (Original) The memory device or the memory circuit as claimed in claim 43, wherein information is rewritten by inverting the magnetization of the ferromagnetic source or the ferromagnetic drain.

58. (Original) A memory device comprising:

first and second transistors that are as claimed in claim 1;

a first line that collectively connects the gate electrode of the first transistor and the gate electrode of the second transistor;

a second line that is connected to a first ferromagnetic drain of the first transistor;

a third line that is connected to a second ferromagnetic drain of the second transistor; and

a fourth line that grounds the ferromagnetic source that is shared between the first and second transistors.

59. (Original) A memory circuit comprising

memory cells that are formed with the memory devices as claimed in claim 58, the memory cells being arranged in a matrix fashion.

60. (Original) The transistor as claimed in claim 1, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor.

61. (Canceled)

62. (Previously Presented) The transistor as claimed in claim 1, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor, the transistor being of the accumulation channel type.

63. (Original) The transistor as claimed in claim 5, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor, the transistor being of the inversion channel type.

64. (Original) The transistor as claimed in claim 1, wherein a channel length that is defined as the length in the carrier conducting direction in the semiconductor layer or the distance between the ferromagnetic source and the ferromagnetic drain is so short that the semiconductor layer can conduct carriers in a ballistic manner, or the channel length is equal to or shorter than the mean free path associated with carrier energy relaxation.

65. (Original) The transistor as claimed in claim 1, further comprising

a metal layer that forms a Schottky junction between the semiconductor layer and the metal layer, or a semiconductor layer that forms a Schottky junction between the ferromagnetic metal and the semiconductor layer, or a metal/semiconductor Schottky junction layer,

the metal layer, the semiconductor layer, or the metal/semiconductor Schottky layer being formed at the interface between the ferromagnetic metal and the semiconductor layer.

66. (Canceled)

67. (Original) The transistor as claimed in claim 60, wherein, when the relative magnetization of the ferromagnetic drain with respect to the ferromagnetic source is

antiparallel magnetization, the drain current is lower than the drain current in a case of parallel magnetization.

68. (Previously Presented) The transistor as claimed in claim 60, wherein transconductance can be controlled in accordance with the relative magnetization direction_of the ferromagnetic drain with respect to the ferromagnetic source.

69. (Previously Presented) A memory device comprising

the transistor as claimed in claim 60,

using the transistor, information being stored in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source,

the information stored in the transistor being detected based on the transconductance of the transistor depending on the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source.

70. (Original) The memory device as claimed in claim 42, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor.

71. (Original) The memory circuit as claimed in claim 50, wherein the semiconductor layer is an undoped semiconductor or an intrinsic semiconductor.

72. (Currently Amended) A transistor comprising:

a source and a drain that are of a first conduction type, and are formed with ferromagnetic semiconductors;

a semiconductor layer that is provided associated with the source and the drain, and has a channel of the first conduction type formed therein; and

a gate electrode that is formed as opposed to the semiconductor layer.

wherein the ferromagnetic semiconductors in the source and the drain are directly contacted with the ~~semiconductor layer~~channel.

73. (Original) The transistor as claimed in claim 72, wherein the semiconductor layer is formed with an undoped semiconductor or an intrinsic semiconductor.

74. (Original) The transistor as claimed in claim 72, wherein a channel length that is defined as the length in the carrier conducting direction in the semiconductor layer or the distance between the ferromagnetic source and the ferromagnetic drain is so short that the semiconductor layer can conduct carriers in a ballistic manner, or the channel length is equal to or shorter than the mean free path associated with carrier energy relaxation.

75. (Previously Presented) A transistor comprising:

a source that is formed with a first pn junction between a first ferromagnetic semiconductor and a semiconductor layer that are of different conductive types from each other;

a drain that is formed with a second pn junction between a second ferromagnetic semiconductor and the semiconductor layer that are of different conductive types from each other; and

a gate electrode that is formed associated with the semiconductor layer,

wherein the first ferromagnetic semiconductor and the second ferromagnetic semiconductor are directly contacted with the semiconductor layer that has different conductive types from the first ferromagnetic semiconductor and the second ferromagnetic semiconductor.

76. (Original) The transistor as claimed in claim 75, wherein a channel length that is defined as the length in the carrier conducting direction in the semiconductor layer or the distance between the ferromagnetic source and the ferromagnetic drain is of such length that the semiconductor layer can conduct carriers in a ballistic manner, or the channel length is equal to or shorter than the mean free path for carrier energy relaxation.

77. (Original) The transistor as claimed in claim 72, wherein, when the relative magnetization of the ferromagnetic drain with respect to the ferromagnetic source is antiparallel magnetization, the drain current is lower than the drain current in a case of parallel magnetization.

78. (Previously Presented) The transistor as claimed in claim 72, wherein transconductance can be controlled in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source.

79. (Previously Presented) A memory device comprising

the transistor as claimed in claim 72,

using the transistor, information being stored in accordance with the relative magnetization direction_of the ferromagnetic drain with respect to the ferromagnetic source,

the information stored in the transistor being detected based on the transconductance of the transistor depending on the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source.

80. (Original) The memory device as claimed in claim 42, wherein the a source and a drain that are of a first conduction type, and are formed with ferromagnetic semiconductors;

a semiconductor layer that is provided associated with the source and the drain, and has a channel of the first conduction type formed therein; and

a gate electrode that is formed as opposed to the semiconductor layer.

81. (Original) The memory circuit as claimed in claim 50, wherein the a source and a drain that are of a first conduction type, and are formed with ferromagnetic semiconductors;

a semiconductor layer that is provided associated with the source and the drain, and has a channel of the first conduction type formed therein; and

a gate electrode that is formed as opposed to the semiconductor layer.

82. (Canceled)

83. (Original) The transistor as claimed in claim 1, wherein a gate insulating film formed between the gate electrode and the semiconductor layer is an insulator that is formed through oxidization or deposition.

84. (Original) The transistor as claimed in claim 83, wherein the gate insulating film contains a high dielectric constant material.

85. (Original) The transistor as claimed in claim 1, wherein the transistor is a MISFET.

86. (Original) The transistor as claimed in claim 1, wherein an impurity is added to the semiconductor layer, so that the transistor functions as a depletion-mode transistor.